REMARKS

Claims 1-20, 22 and 24 were pending. No claims have been amended. No claims have been added/canceled. Accordingly, claims 1-20, 22 and 24 remain pending subsequent entry of the present amendment.

Prior Rejections

Applicant notes and appreciates the withdrawal of the prior rejections based upon the Park reference.

35 U.S.C. § 112 Rejections

In the present Office Action, claims 1 and 17 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner states:

> "Claims 1 and 17 claims validating predicted information. It is unclear as to how predicted information is validated and what the predicted information is validated against." (Office Action, page 2).

The predicted information is validated against the history record for that packet stored in MEM 204, which is shown in Figures 2 and 3. The process for validation may include buffer logic 205 comparing the predicted information with the historical component and a preset threshold variable.

In the Description, the above features are described in at least paragraphs 0029 – 0040. Specifically, regarding what the predicted information is validated against, the Specification recites:

> "In one example, buffer logic 205 is enhanced with a responsibility of validating a prediction based on access of MEM 204 of predictor 202 after an arbitrary prediction is made." (Description, paragraph 0037).

The contents of MEM 204 are described in the Specification in the following:

> "Packet predictor 202 has, in this example, a dedicated memory (MEM) 204 provided therein and adapted to store historical data regarding real data packets previously processed within the system and historical data about successful instances of predicted data packets within the system …
>
> For example, MEM 204 may store historical data covering the last 10 data packets received, and also the practical result of the last ten data packets predicted." (Description, paragraphs 0029-0030).
>
> "In one embodiment, the historical data could be componential such that each predictable component category has its own constantly changing variable. Each component variable can be probability-based and weighed against a preset threshold." (Description, paragraph 0035).

Regarding how predicted information is validated, the Description discloses:

> "In this way, variables with a high likelihood of materializing in the next packet could be included in a prediction. In another embodiment, an algorithm is run that incorporates the sum weight of all of the component variables and produces a single predictive variable that is weighed against a preset threshold value for initiating or not initiating a total packet prediction" (Description, paragraph 0035).
>
> "In this embodiment, logic provided within buffer logic 205 runs an algorithm comparing the predicted information (the only information in queue at this point) with the historical variable and a preset threshold variable. The buffer logic then decides whether to accept or to invalidate the prediction …
>
> It is noted herein that a commitment to processing the predicted information is based on a comparison of the predicted information to the current value of the historical data and subject in a preferred embodiment to an acceptance or non-acceptance threshold. This algorithm can be run either by buffer logic 205, or by packet predictor

> 202 without departing from the spirit and scope of the present invention.
>
> In the first case scenario, predictions are attempted for every next packet based on the last known history data before update. The buffer logic can, however, invalidate a prediction if its comparison with historical data detects that the prediction would likely be in error or does not meet a pre-set value threshold." (Description, paragraphs 0037-0039).

The predicted information, itself, may comprise header information such as "source information, destination information, packet flow information, data protocol information, packet size information, and media type information". In one embodiment, the predicted information is validated at the time of receipt of a real data packet as just described, but in another embodiment, it may be validated later. Concerning the contents of the predicted information, the Description provides:

> "For example, header information includes typically some or all of source information, destination information, packet flow information, data protocol information, packet size information, and media type information. Each of these components of information in the header of a data packet can be regarded as a separate predictable component. Moreover, some of these components share dependencies. For example a header of two separate packets having a same source and destination address arriving in a close time period are quite likely to be of the same packet flow. Packets of a same flow are further quite likely to be of a same size. Packets of a same flow are also likely to be of a same protocol such as UDP or TCP/IP and so on." (Description, paragraph 0033).

Applicant submits the above recitations describe "how predicted information is validated and what the predicted information is validated against." Therefore, claims 1 and 17 contain subject matter, which was described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

35 U.S.C. § 102 Rejections

In the present Office Action claims 1, 9 and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by newly cited reference Matic, et al. ("Predictive Playout Delay Adaptation for Voice over Internet") (hereinafter "Matic"). However, Applicant submits each of the pending claims recite features neither disclosed nor suggested by the cited art. Accordingly, Applicant traverses the above rejections and requests reconsideration.

Claim 1 recites a packet buffering system that comprises:

> "…a packet predictor, coupled to said at least one input port, for predicting information about a future packet in any one of the plurality of data flows based on history of previously received packets from the plurality of data flows, said history stored in a memory coupled to said packet predictor;
> a plurality of queues for storing packets received from said plurality of sources, and for storing said predicted information about said future packet." (emphasis added).

As highlighted above, claim 1 recites "a plurality of queues for storing packets received from said plurality of sources". In the present Office Action, the Examiner states the above features are disclosed in the Abstract of Matic which describes:

> "Receiver also keeps a record of all relevant packet information in a text file that is used as an input to a delay jitter predictor."

Therefore, Matic discloses packet information is stored in a text file. A text file is not a plurality of queues and is not equivalent to a plurality of queues. Applicant has also reviewed the remainder of Matic and the above highlighted features are nowhere found. Applicant further notes the recitation concerning a plurality of queues appears multiple times in the claim. As Matic nowhere discloses or suggests these features, claim 1 is patentably distinguishable from the cited art. Independent claim 9 is distinguishable for similar reasons.

In addition to the above, claim 1 recites "direction logic, coupled to said packet predictor, for generating a Packet ID for said future packet, wherein said Packet ID is stored in one of said plurality of queues." However, Matic does not disclose these features. In the present Office Action, the examiner states the following:

> "(Matic teaches id for the packet and storage of the packets within vectors. ID that is to be used by a computing system must inherently store the id. Section 3, p. 350, subsection A [Learning], Matic)." (Office Action, page 4, para. 1).

The portion of Matic cited by the examiner is reproduced below:

> "We can treat a problem of jitter prediction like nonlinear system identification. We need to extract dynamic process model to predict x(t) using past two candidates x(t-2) and x(t-1). For a learning process we have to reformat our training data shown in Fig. 2. All the captured interarrival times are placed in a vector j(n), n=1, 2, ..., 5000. Hence, for the learning purpose we present this data in a form given in (9) … Format needed for training is a vector where all members are inputs, except the last one that is an output
>
> $$[x(t-2),x(t-1);x(t)], \qquad (9)$$
>
> where values x(t-2) and x(t-1) represent inputs and x(t) is an output." (Matic, page 350, para. 2). (emphasis added).

Concerning the learning process for the neural network Adaptive Neuro-Fuzzy Inference System (ANFIS), Applicant has reviewed the above disclosure and the remainder of the cited reference and submits there is no disclosure of direction logic "for generating a Packet ID for said future packet".

Further, the reference does not disclose storing the generated ID of a future packet as recited. As seen in the disclosure above, Matic teaches "captured interarrival times are placed in a vector".

In addition, setting aside the absence in the reference of a generated ID of a future packet, it is suggested that the packet ID storage is inherent. It is first noted that while the examiner makes reference to "the packet ID" in Matic, the reference itself makes no mention of a packet ID. Therefore, it is not clear to what packet ID the examiner is referring. Consequently, as there is no disclosure of a packet ID in Matic, Applicant does not find storage of the packet ID to be inherent as suggested.

Additionally, claim 1 recites "buffer logic, coupled to said packet predictor, for accessing said memory and for validating said predicted information about said future packet based on said access to said memory". Applicant has reviewed the cited reference and submits Matic nowhere discloses the above features. Again, the examiner cites the above mentioned disclosure of Matic (p. 350, subsection A). However, Applicant finds no such disclosure therein. In the Learning subsection there is no mention of "validating said predicted information about said future packet based on said access to said memory" or any other kind of validating. For at least these additional reasons, claim 1 is patently distinct from the cited art.

Furthermore, claim 1 recites validation is needed prior to speculative processing: "if said buffer logic validates said predicted information, notification is made to said direction logic which passes said Packet ID for said future packet to said processing core to initiate speculative processing". As stated above, Matic on pages 349-350, Section III, nowhere discloses validation of any kind much less validation prior to speculative processing. The output x(t), which is the predicted interarrival time of a future packet, is calculated for each three consecutive member set. No sets are skipped due to invalidation of information in x(t-2) or x(t-1). Thus, claim 1 is believed to be patentably distinct from the cited art. Claim 17 is distinguishable for similar reasons.

Finally, the dependent claims recite additional features not disclosed or suggested by the cited art. As an example, claims 6 and 15 recite the features:

> "…said packet predictor predicts specific characteristics, comprising one or more of packet type, packet flow identification, sender information, destination information, and packet size for said future packet."

However, Matic nowhere discloses a predictor that predicts the characteristics listed above. Rather, Matic discloses a predictor that predicts the delay jitter of packets. In the present Office Action, the Examiner states the above features are disclosed in the following portion of Matic:

> "To achieve this goal we need to know characteristics of jitter in advance. Hence, main component of smoother on a receiver side is a jitter predictor. In this paper we present one of the possible solutions: the predictor based on Adaptive Neuro-Fuzzy Inference System." (Matic, p. 348, col. 2, paragraph 6).

Only prediction of jitter is disclosed above and not prediction of any of the characteristics recited in the claim. Accordingly, claims 6 and 15 are patentably distinct from Matic for these additional reasons as well.

Applicant believes all claims to be patentably distinguished from the cited art for at least the above reasons.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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